REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of this application is requested. Claims 1-24 are now pending with claims 1, 16, and 19 being independent. Claims 1, 4, 19, and 24 have been amended.

The specification has been amended on page 2, line 6 to provide the serial number of the co-assigned application and to remove attorney docket numbers. The specification has been further amended to claim priority to a provisional application in the first paragraph of the specification. No new matter has been introduced.

Claim 24 has been amended in response to the Examiner's objection in paragraph 7 of the Office Action mailed December 4, 2003.

Claims 1 and 19 have been amended to correct punctuation errors and minor informalities.

Claim 1 describes a digital signal processing (DSP) system that includes a shared program memory and a plurality of processor subsystems coupled to the shared program memory to concurrently access instructions stored by the shared program memory. The shared program memory is conditionally write-protected from at least one of the processor subsystems.

Claims 1-15 stand rejected under 35 U.S.C. § 102(e) as anticipated by Hedayat et al. (6,327,648). Applicants request reconsideration and withdrawal of this rejection for at least the reason that Hedayat does not describe or suggest a shared program memory. Hedayat also does not describe or suggest a plurality of processor subsystems coupled to the shared program memory to concurrently access instructions stored by the shared program memory.

Hedayat, as shown in Figure 3 and described in the Abstract, teaches a DSP system with a main DSP 100 that operates concurrently with an auxiliary DSP 200 for implementing a filter algorithm. The main DSP 100 and auxiliary DSP 200 have separate program memories 102 and 202, respectively, but share the same data memory 300. The auxiliary DSP program memory 202 is mapped to the main DSP program memory 102 to allow the main DSP 100 to download filter process instructions from its program memory 102 into the auxiliary DSP program memory 202. The auxiliary DSP 200 fetches the instructions from its program memory 202 to execute them. The auxiliary DSP 200 is prevented from access to the shared data in the data memory 300

when this memory is being used by the main DSP 100. An arbitration mechanism gives the auxiliary DSP 200 access to the data memory 300 only when the main DSP 100 is not using the data memory 300. Thus, in Hedayat, the data memory 300 cannot be accessed by the auxiliary DSP 200 and the main DSP 100 concurrently and so the filter process instructions cannot be executed concurrently by the auxiliary DSP and main DSP as one DSP must be halted while the other DSP is accessing and executing instructions that use the shared data memory. Col. 4, lines 50-52 describes preventing the auxiliary DSP 200 from fetching instructions from its program memory 202 when the program memory is accessed by the main DSP 100. The main DSP 100 supplies the auxiliary DSP 200 with a program memory busy signal to prevent the auxiliary DSP 200 from fetching instructions. Main DSP 100 accesses auxiliary DSP program memory 202 to download filter process instructions as described in col. 5, lines 43-54. Thus, the main DSP 100 and auxiliary DSP 200 do not concurrently access instructions stored in a shared program memory. For at least these reasons, Applicants respectfully submits that claim 1 is patentable over Hedayat.

Claims 2-15 depend from independent claim 1. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claim 2-15 for at least the reasons discussed above with respect to claim 1.

Amended claim 4 recites that the processor subsystems are allowed to write information to the shared program memory to test the digital signal processing system while the processor subsystems are in an emulation mode. Applicants request reconsideration and withdrawal of the rejection of claim 4 for the further reason that Hedayat does not describe or suggest that the processor subsystem writes information to the shared program memory to test the digital signal processing system. In Hedayat, as described in col. 3, lines 46-59, the main DSP 100 downloads filter process instructions to auxiliary DSP program memory 202 for execution by auxiliary DSP 200 so that the main DSP 100 can support other tasks. Separate operations of the main and auxiliary DSPs in Hedayat improve the speed of digital data processing. Hedayat does not describe or suggest that the processor subsystem writes information to the shared program memory to test the digital signal processing system. For at least this additional reason, Applicants respectfully submit that claim 4 is patentable over Hedayat.

Claim 16 describes a method of conditionally write protecting a shared program memory in a multi-core processor chip. The method comprises receiving a requested shared program memory access operation from a processor core. The method also includes combining the requested shared program memory access operation with a signal indicative of a current operating mode to produce a communicated shared program memory access operation, wherein when the current operating mode is a normal operating mode, the communicated shared program memory access operation is prevented from being a write operation.

Claims 16-18 stand rejected under 35 U.S.C. § 102(e) as anticipated by Hedayat. Applicants request reconsideration and withdrawal of this rejection for at least the reason that, as discussed above, Hedayat does not describe or suggest a shared program memory in a multi-core processor chip. Hedayat teaches a main DSP 100 and auxiliary DSP 200 having separate program memories 102 and 202, respectively, but sharing the same data memory 300. For at least the reasons discussed above, Applicants respectfully submit that claim 16 is patentable over Hedayat.

Claims 17-18 depend from independent claim 16. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 17-18 for at least the reasons discussed above with respect to claim 16.

Amended claim 19 describes a digital signal processor chip that includes a volatile memory containing software instructions and a plurality of processor cores coupled to the volatile memory via a corresponding plurality of instruction buses. The processor cores are configured to retrieve and execute instructions from the volatile memory. Each of the instruction buses is configured to convey only read operations to the volatile memory while their corresponding processor cores are in a normal operating mode.

Claims 19-23 stand rejected under 35 U.S.C. § 102(e) as anticipated by Hedayat. Applicants request reconsideration and withdrawal of this rejection for at least the reason that, as discussed above, Hedayat does not describe or suggest that the processor cores are configured to retrieve and execute instructions from the volatile memory. In Hedayat, as described in the Abstract, the auxiliary DSP program memory 202 is mapped to the main DSP program memory 102 to allow the main DSP 100 to download filter process instructions from its program memory 102 into the auxiliary DSP program memory 202. The auxiliary DSP 200 fetches the

instructions from its program memory 202 to execute them. The main DSP 100 does not retrieve or execute filter process instructions from the auxiliary DSP program memory 202. Thus, Hedayat does not describe or suggest that the processor cores are configured to retrieve and execute instructions from the volatile memory. Col. 5, lines 46-50 in Hedayat teaches the main DSP 100 downloading filter process instructions from its program memory 102 to the auxiliary DSP program memory 202. The auxiliary DSP 200 then fetches these instructions from its program memory 202 to execute them. Hedayat does not describe or suggest that both the auxiliary DSP 200 and the main DSP 100 fetch the filter process instructions from auxiliary DSP program memory 202 to execute them. For at least these reasons and the reasons discussed above, Applicants respectfully submit that claim 19 is patentable over Hedayat.

Claims 20-23 depend from independent claim 19. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 20-23 for at least the reasons discussed above with respect to claim 19.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as obvious over Hedayat et al. (6,327,648) further in view of Chauvel et al. (6,430,664). Chauvel describes in the Abstract and shows in Figure 1 a DSP (10) including a single DSP core (12) that accesses internal memory using physical addresses and has an internal MMU (19) which allows the DSP (10) to work with a large virtual address space mapped to an external memory (20). However, Chauvel fails to remedy the failure of Hedayat to describe or suggest that a plurality of processor cores are configured to retrieve and execute instructions from a volatile memory. In Chauvel, the DSP includes only one DSP core (12) that accesses a large virtual address space mapped to an external memory (20). Accordingly, Applicants request reconsideration and withdrawal of the rejection of claim 24 for the reasons discussed above with respect to claim 19.

In view of these remarks and amendments, Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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